FIG. 1

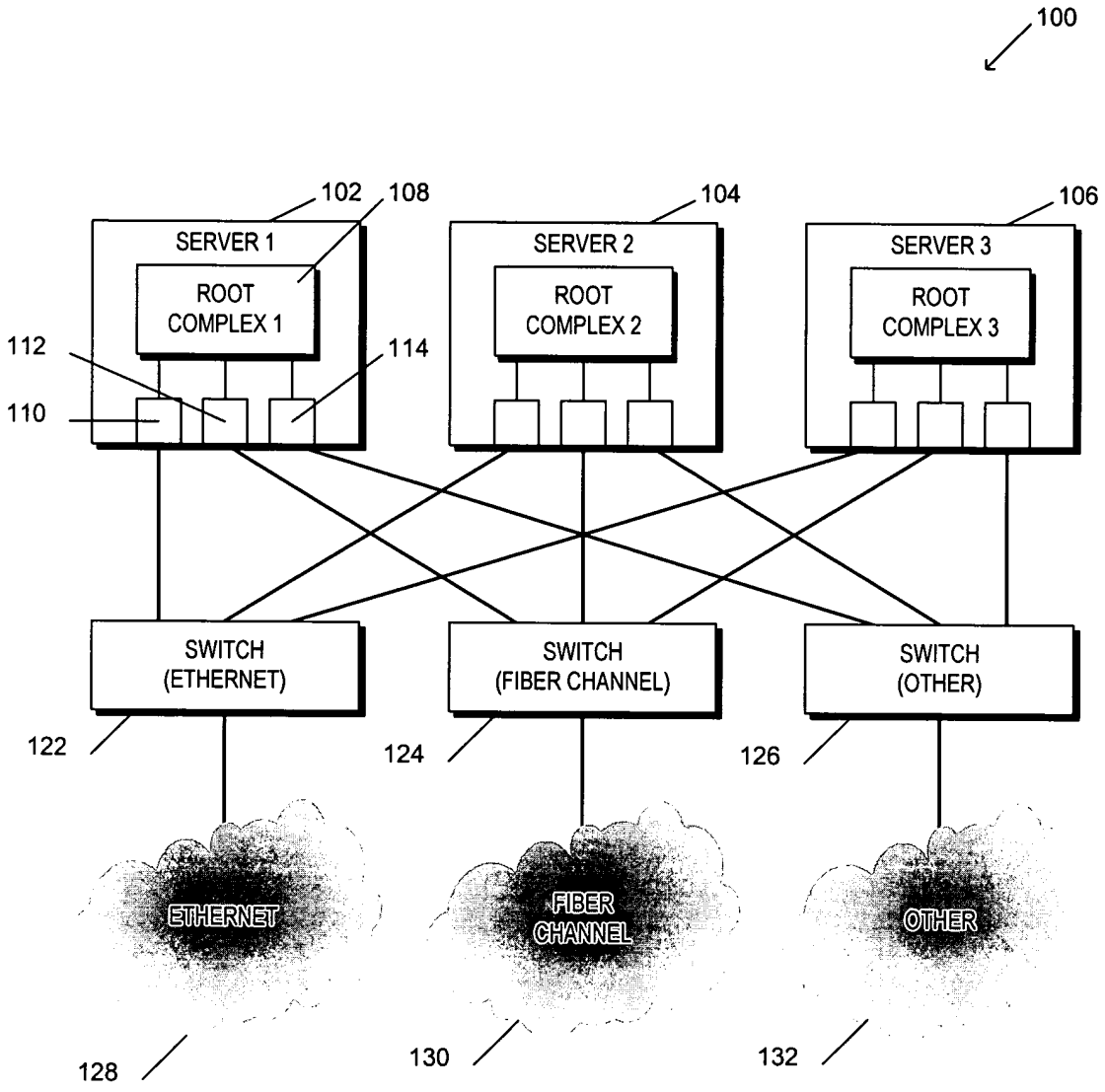

100
102
108
104
106
SERVER 1
ROOT COMPLEX 1
SERVER 2
ROOT COMPLEX 2
SERVER 3
ROOT COMPLEX 3
112
114
110
SWITCH (ETHERNET)
SWITCH (FIBER CHANNEL)
SWITCH (OTHER)
122
124
126
ETHERNET
FIBER CHANNEL
OTHER
128
130
132

FIG. 2A

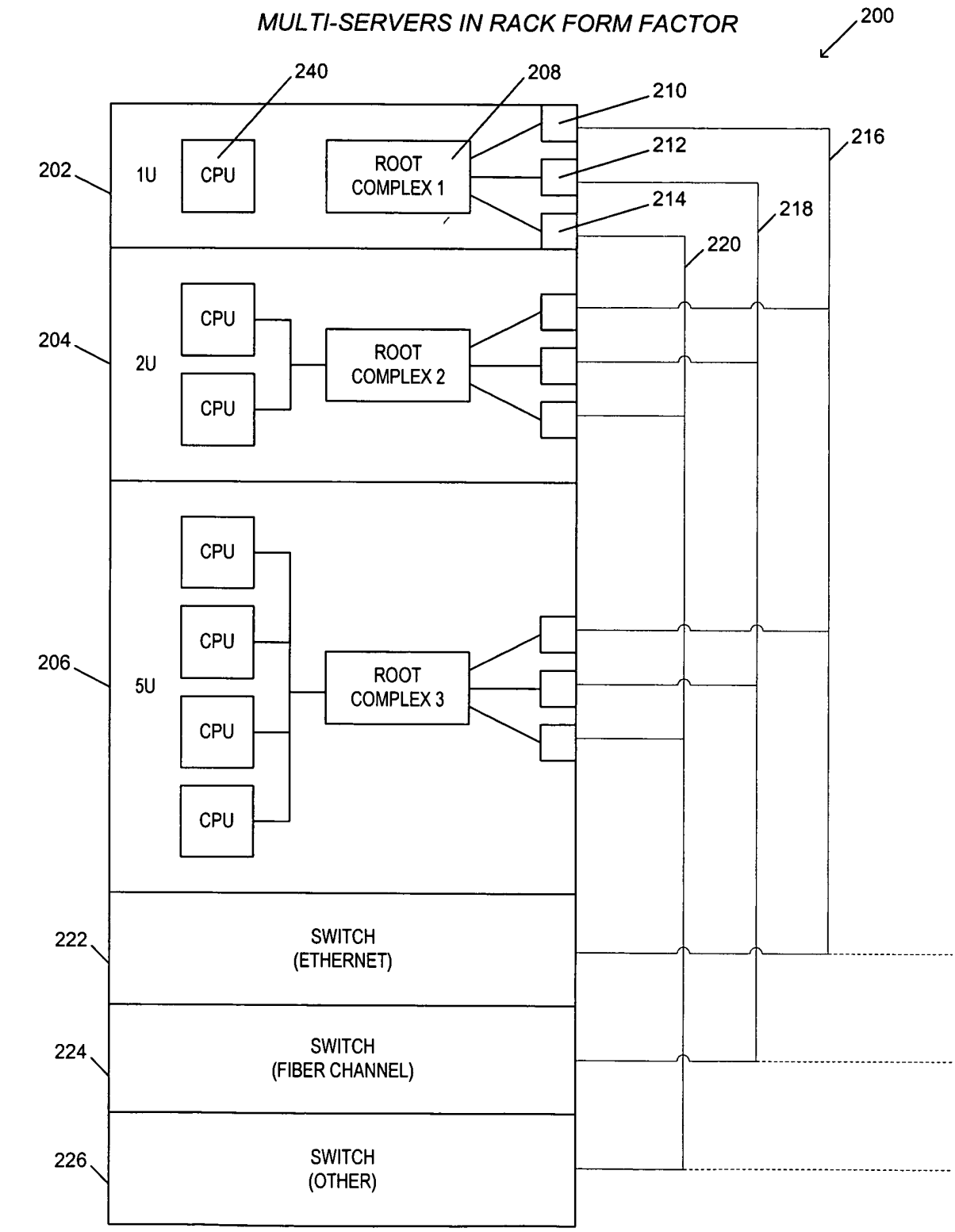

MULTI-SERVERS IN RACK FORM FACTOR
200
240
208
210
216
212
202
1U
CPU
ROOT COMPLEX 1
214
218
220
CPU
204
2U
ROOT COMPLEX 2
CPU
CPU
206
5U
CPU
CPU
ROOT COMPLEX 3
CPU
CPU
222
SWITCH (ETHERNET)
224
SWITCH (FIBER CHANNEL)
226
SWITCH (OTHER)

FIG. 2B

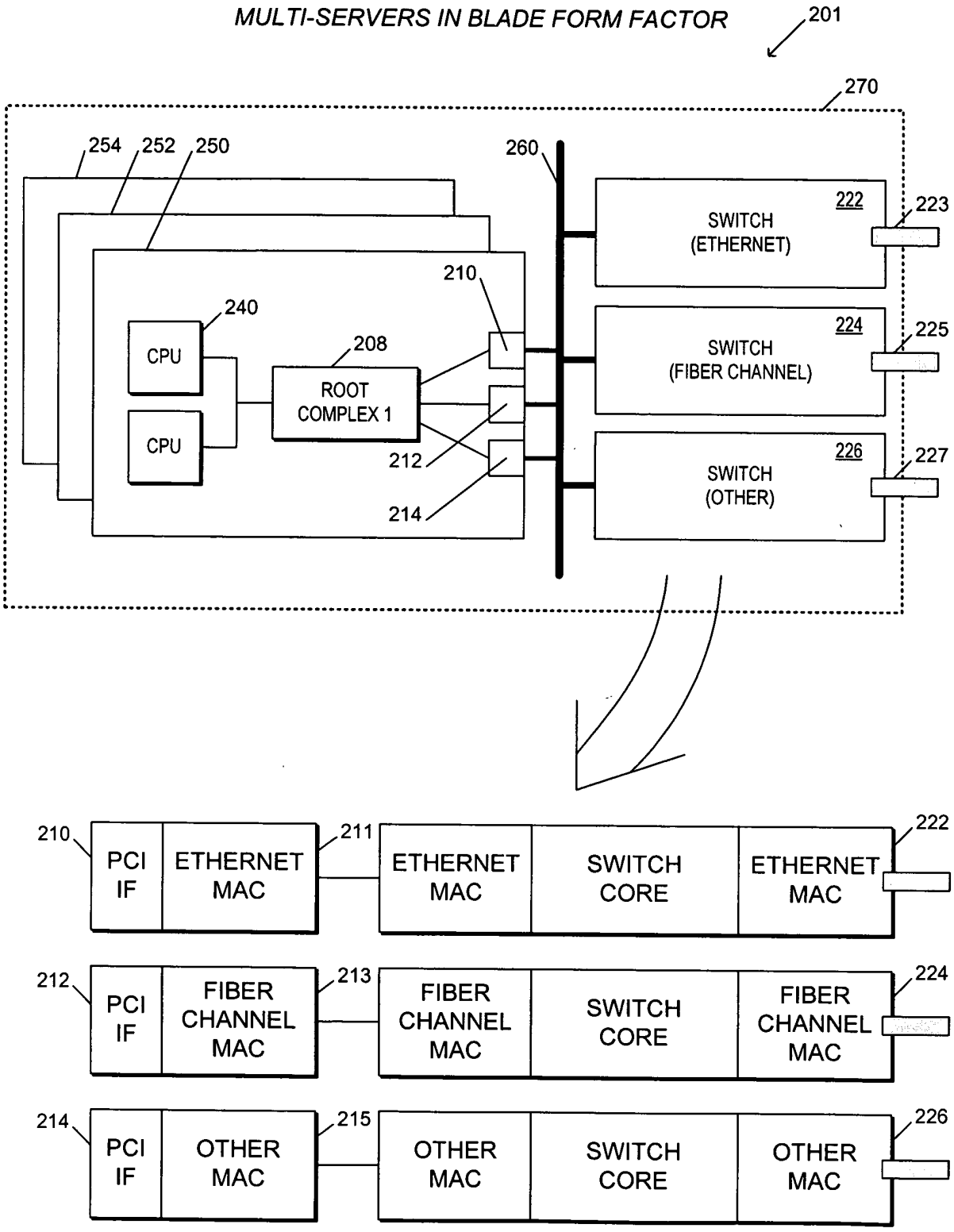

MULTI-SERVERS IN BLADE FORM FACTOR
201
270
254
252
250
260
210
240
CPU
CPU
208
ROOT COMPLEX 1
212
214
222
SWITCH (ETHERNET)
223
224
SWITCH (FIBER CHANNEL)
225
226
SWITCH (OTHER)
227
210
PCI IF
ETHERNET MAC
211
ETHERNET MAC
SWITCH CORE
ETHERNET MAC
222
212
PCI IF
FIBER CHANNEL MAC
213
FIBER CHANNEL MAC
SWITCH CORE
FIBER CHANNEL MAC
224
214
PCI IF
OTHER MAC
215
OTHER MAC
SWITCH CORE
OTHER MAC
226

FIG. 2C

MULTI-SERVERS IN BLADE FORM FACTOR (IN CHASSIS)

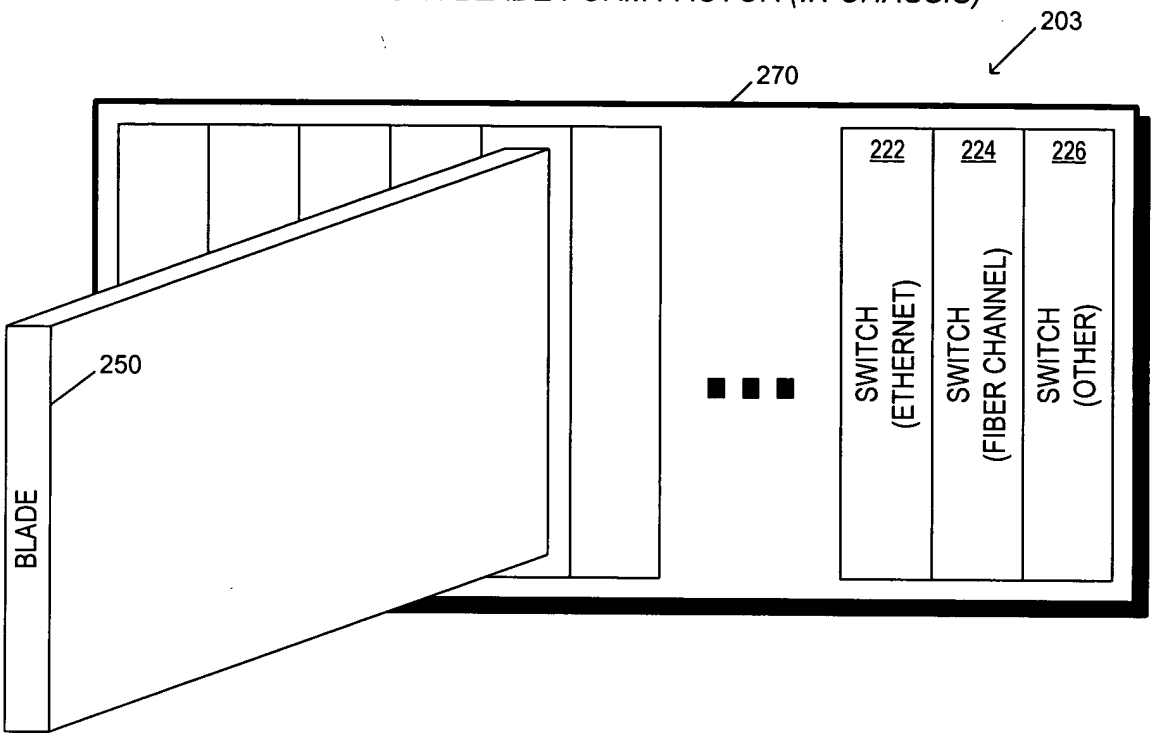


FIG. 3

PCI EXPRESS SERVER ARCHITECTURE

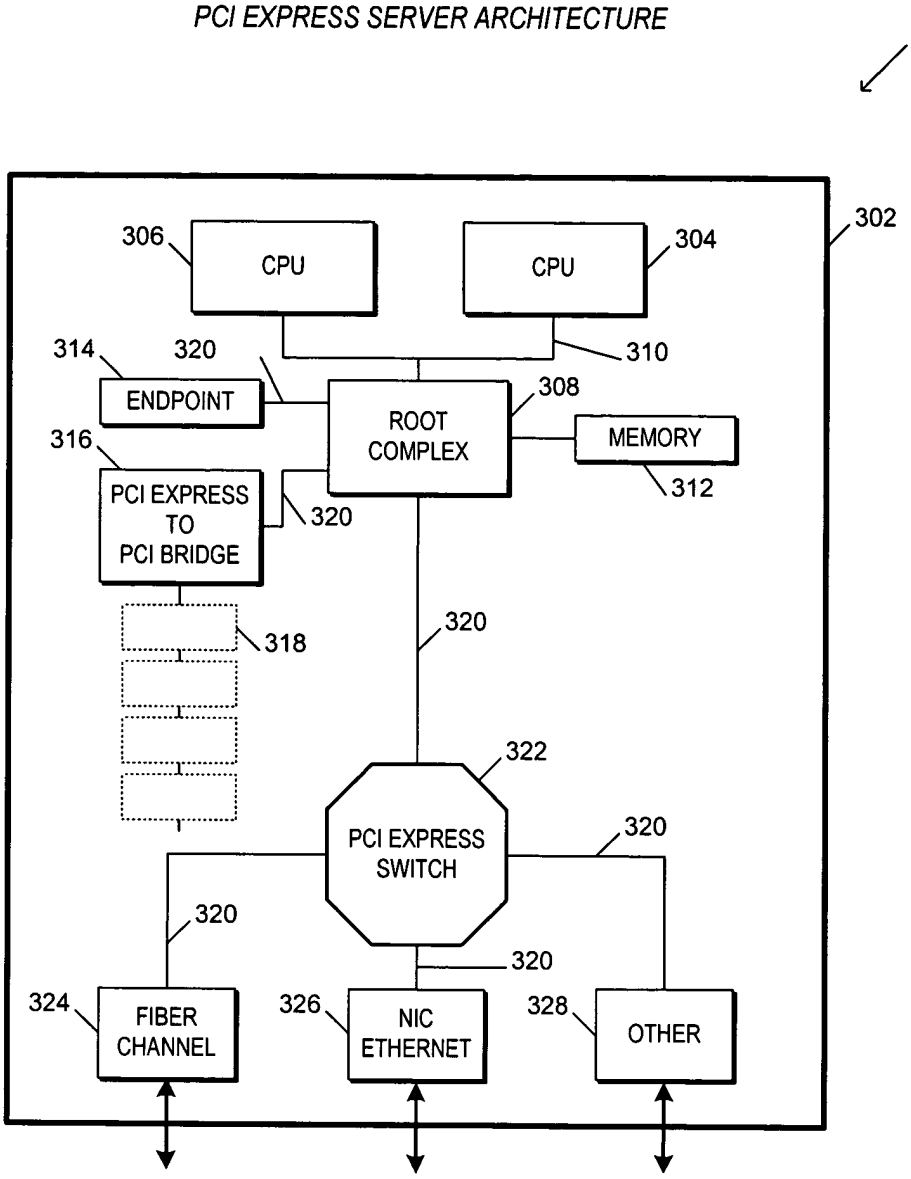


FIG. 4

MULTI-SERVERS IN BLADE FORM FACTOR WITH SHARED I/O SWITCH

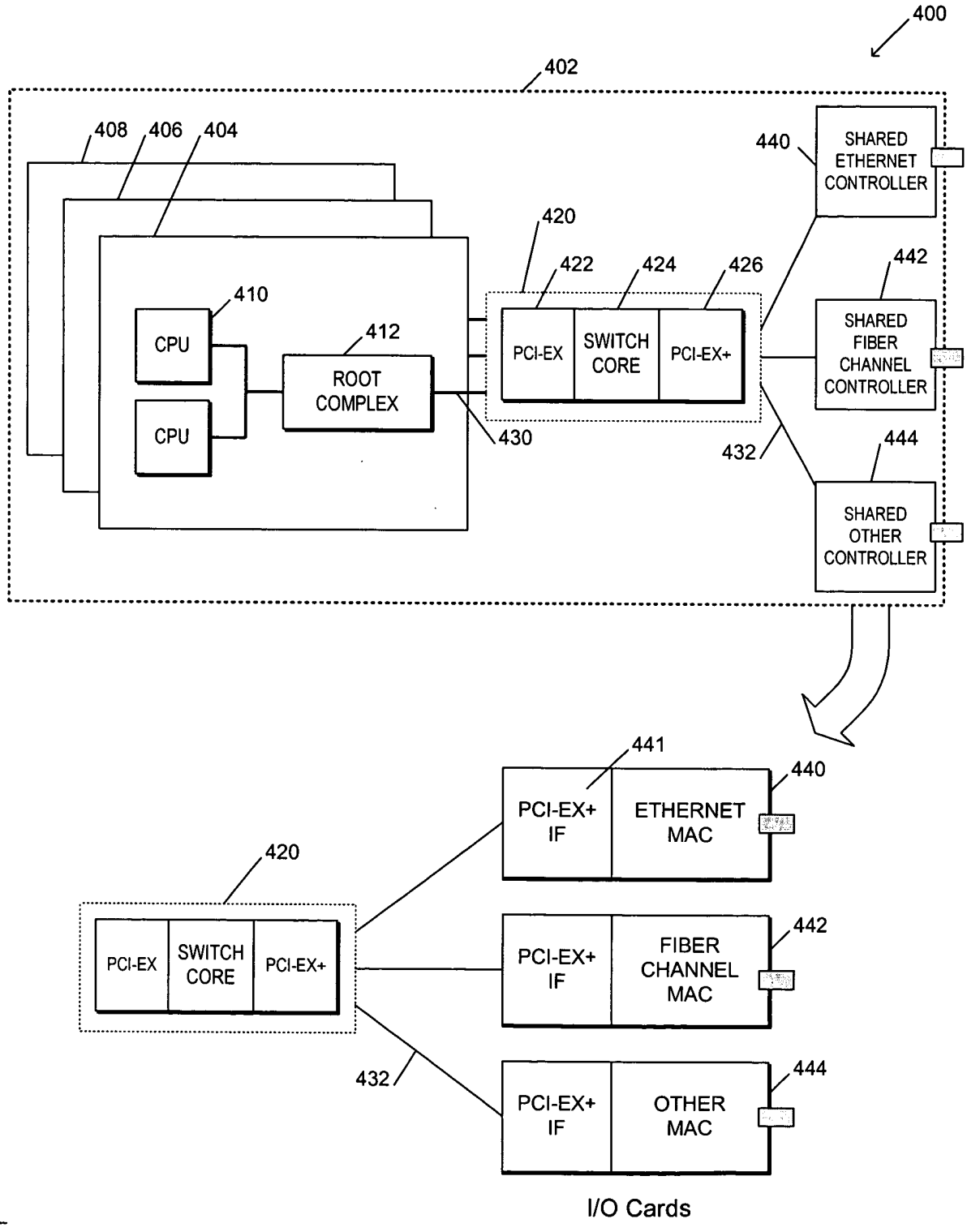


FIG. 5

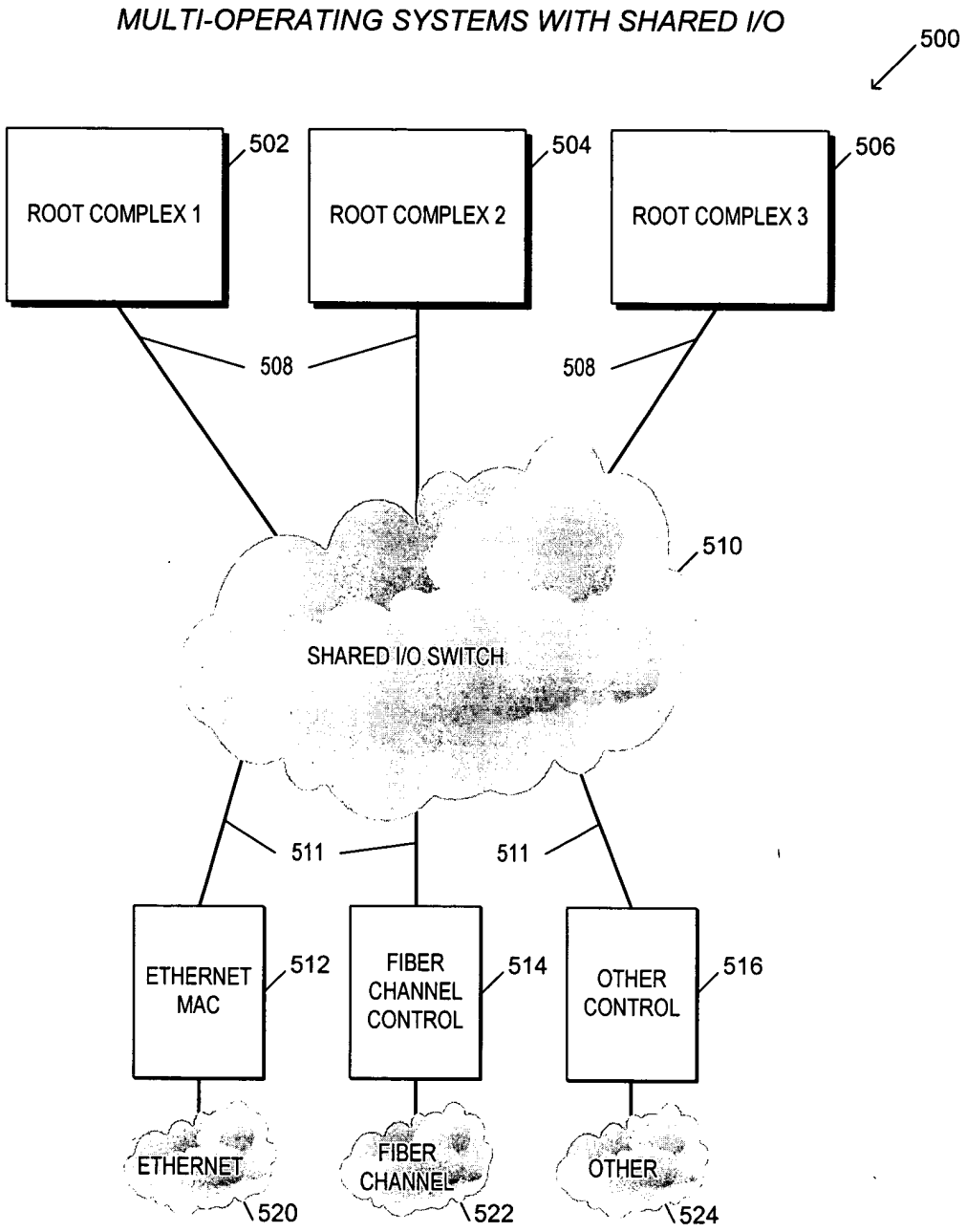

MULTI-OPERATING SYSTEMS WITH SHARED I/O
500
ROOT COMPLEX 1
502
ROOT COMPLEX 2
504
ROOT COMPLEX 3
506
508
508
510
SHARED I/O SWITCH
511
511
ETHERNET MAC
512
FIBER CHANNEL CONTROL
514
OTHER CONTROL
516
ETHERNET
520
FIBER CHANNEL
522
OTHER
524

FIG. 6

MULTI-OPERATING SYSTEMS WITH SHARED ETHERNET CONTROLLER

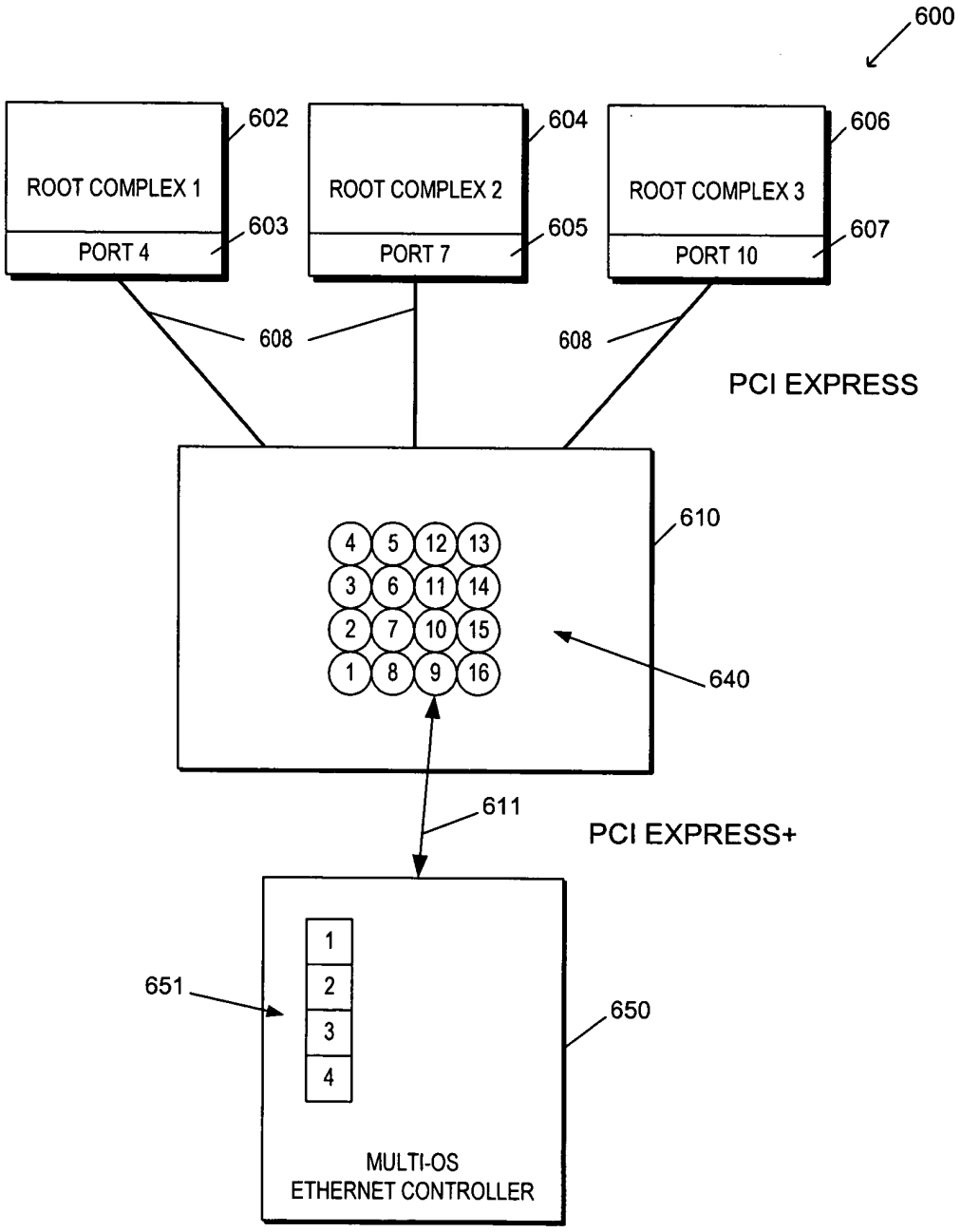


FIG. 7

MULTI-OPERATING SYSTEMS WITH SHARED FIBER CHANNEL CONTROLLER

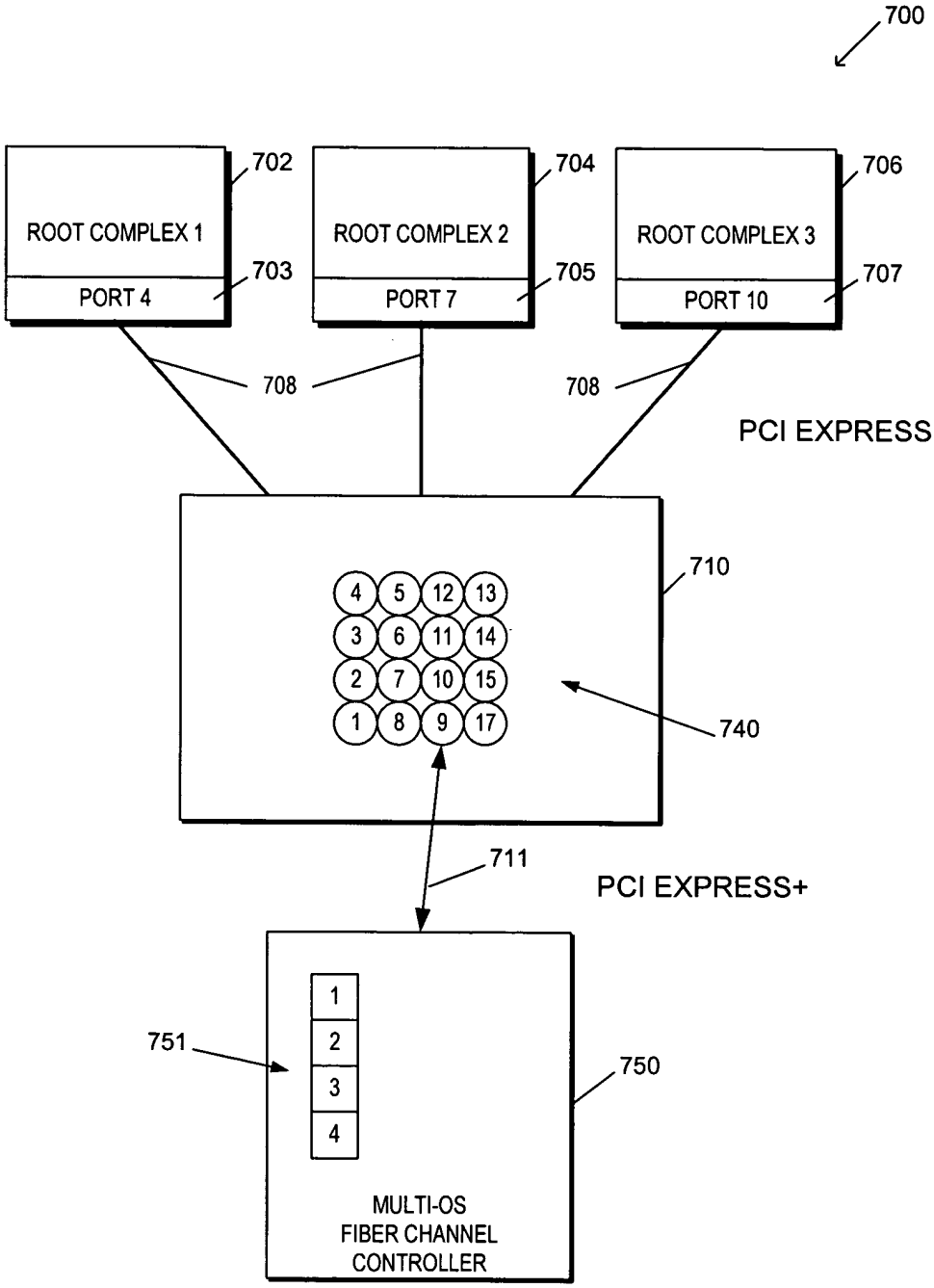


FIG. 8

MULTI-OPERATING SYSTEMS WITH SHARED OTHER CONTROLLER

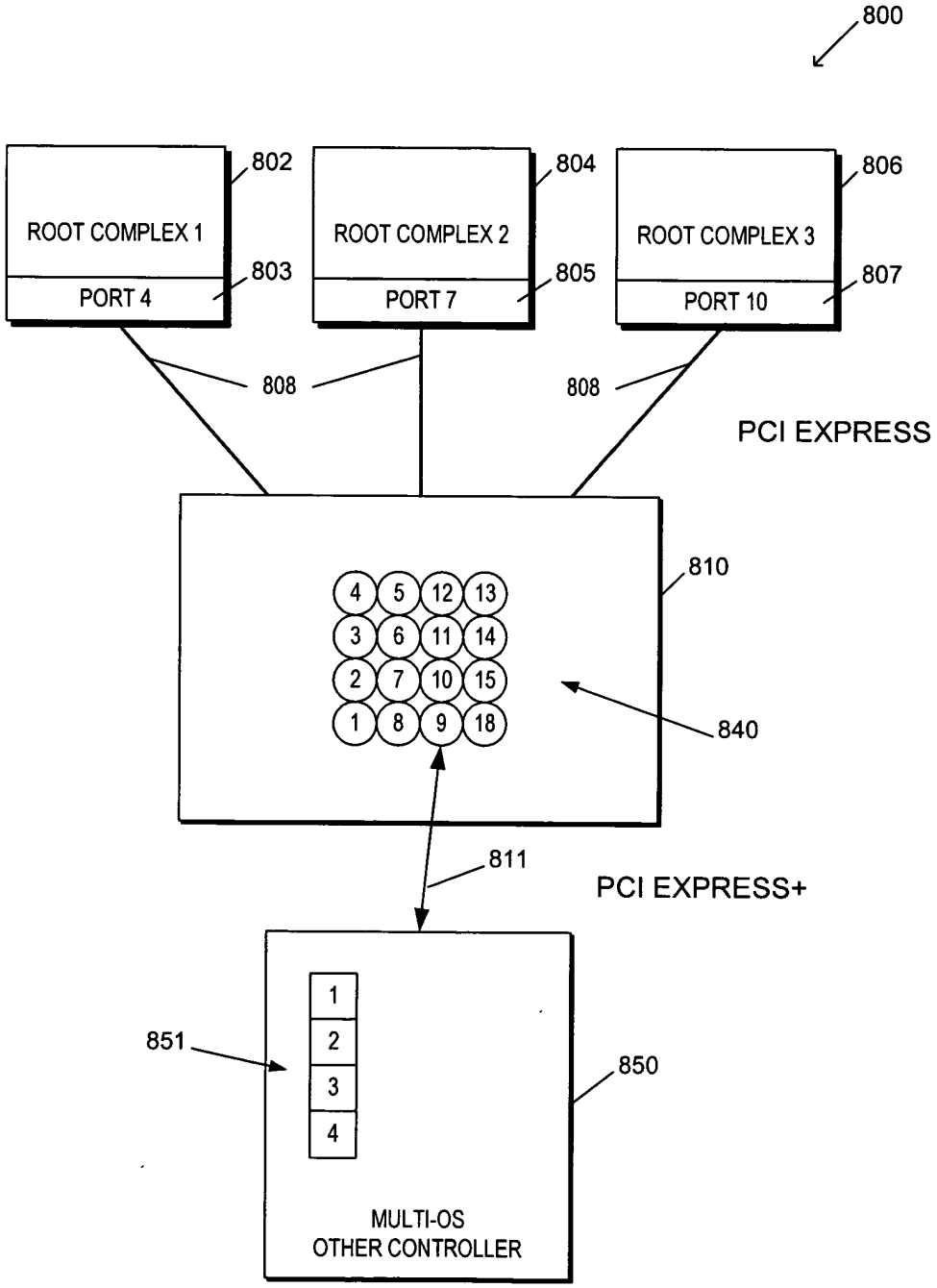


FIG. 9

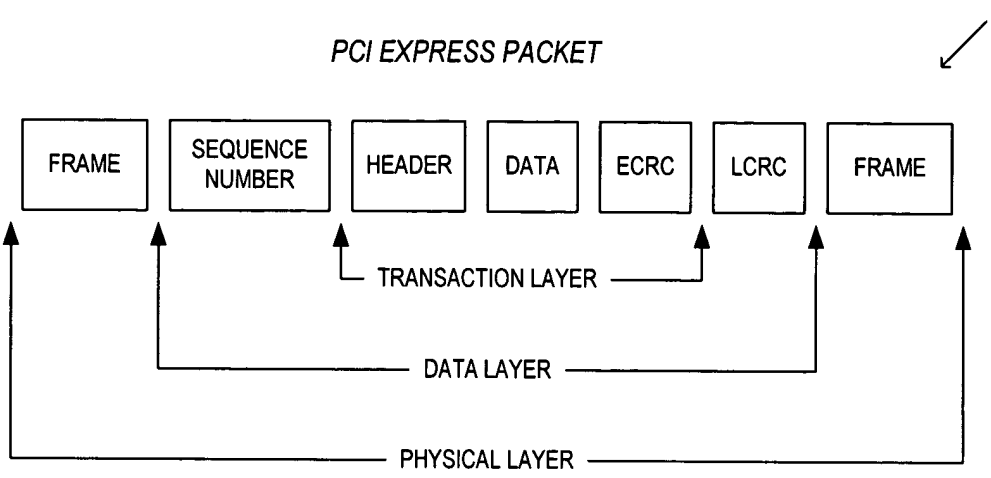


FIG. 10

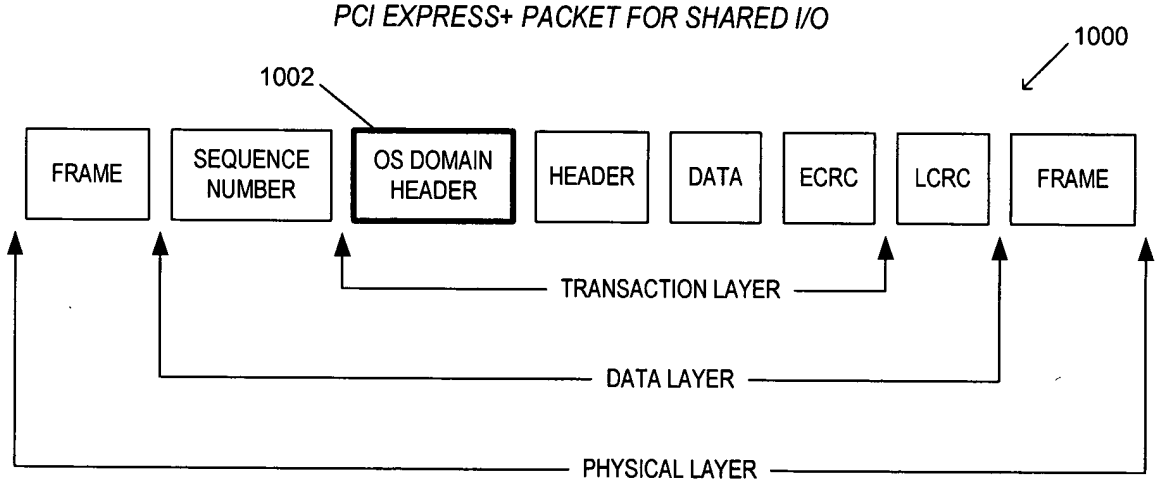
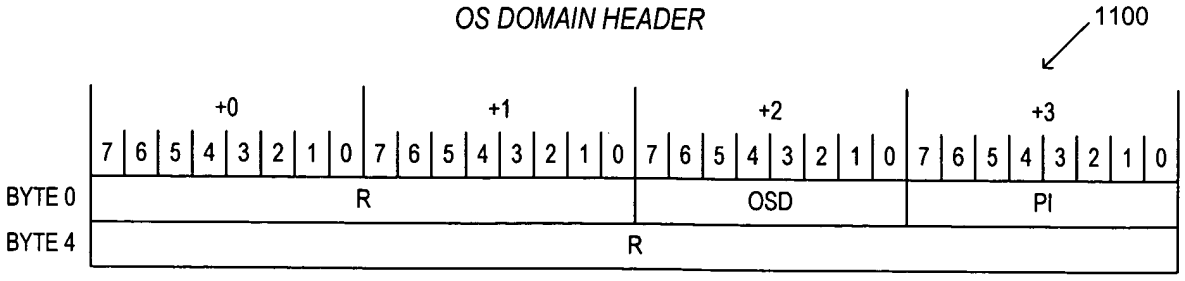


FIG. 11



PI Protocol ID Field

OSD OS Domain Number

R Reserved

FIG. 12 (Prior Art)

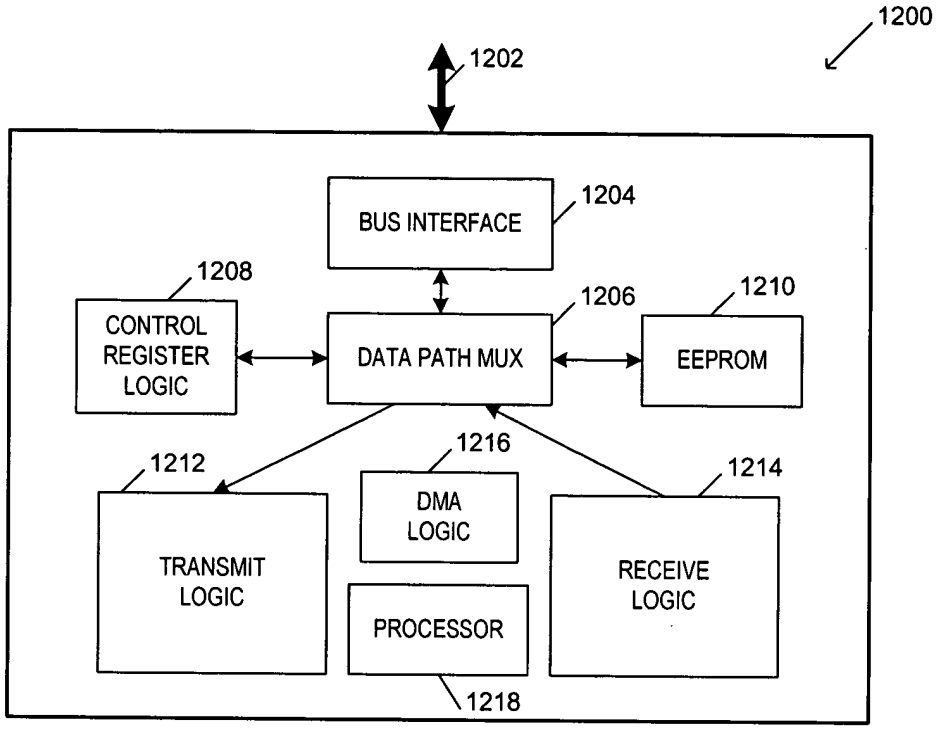


FIG. 13

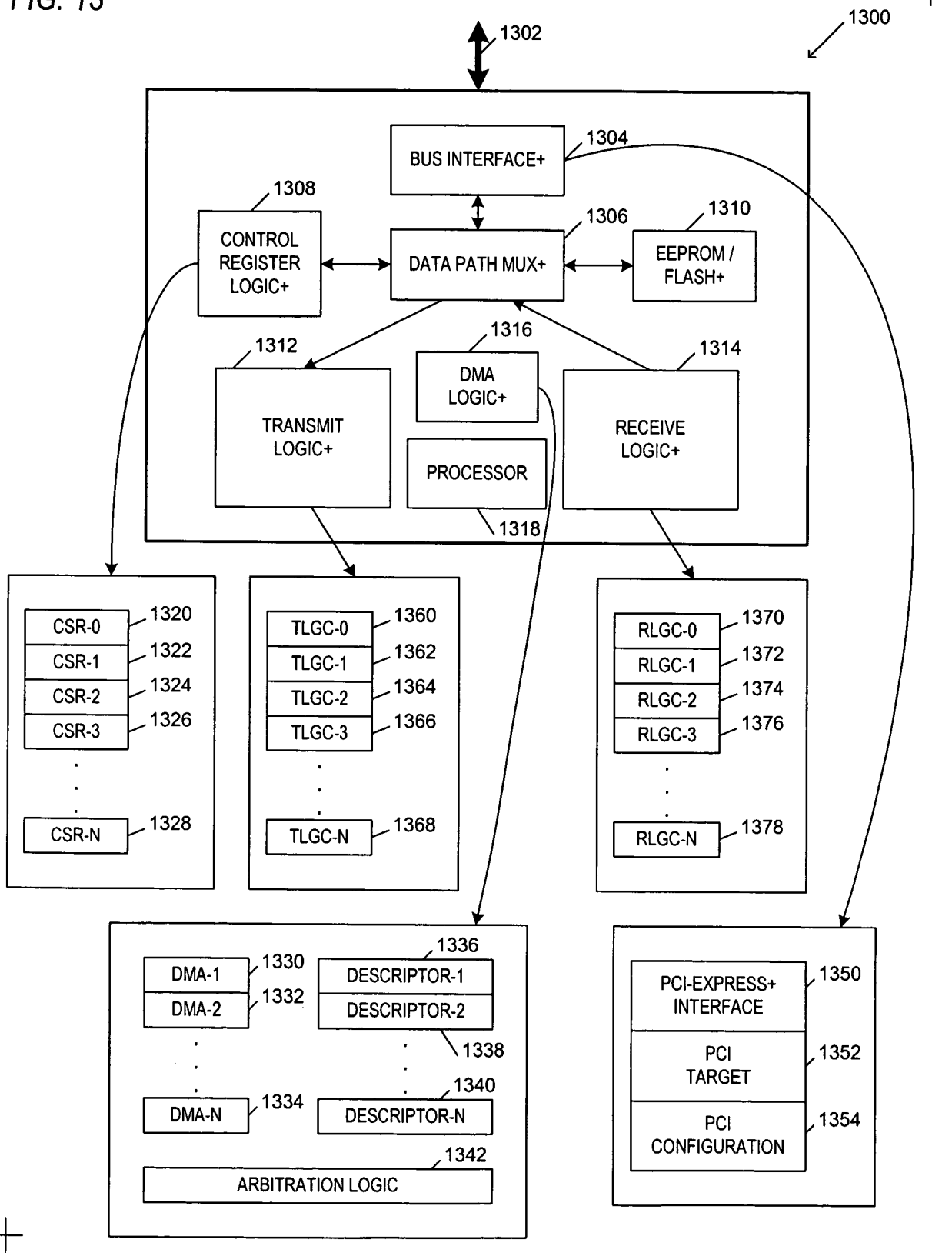

1300
1302
BUS INTERFACE+
1304
1308
CONTROL REGISTER LOGIC+
1306
DATA PATH MUX+
1310
EEPROM / FLASH+
1312
1316
DMA LOGIC+
1314
TRANSMIT LOGIC+
RECEIVE LOGIC+
PROCESSOR
1318
CSR-0
CSR-1
CSR-2
CSR-3
CSR-N
1320
1322
1324
1326
1328
TLGC-0
TLGC-1
TLGC-2
TLGC-3
TLGC-N
1360
1362
1364
1366
1368
RLGC-0
RLGC-1
RLGC-2
RLGC-3
RLGC-N
1370
1372
1374
1376
1378
1336
DMA-1
DMA-2
DMA-N
1330
1332
1334
DESCRIPTOR-1
DESCRIPTOR-2
DESCRIPTOR-N
1338
1340
1342
ARBITRATION LOGIC
PCI-EXPRESS+ INTERFACE
PCI TARGET
PCI CONFIGURATION
1350
1352
1354

FIG. 14

MULTI-OPERATING SYSTEMS WITH SHARED ETHERNET CONTROLLER PACKET FLOW EXAMPLE

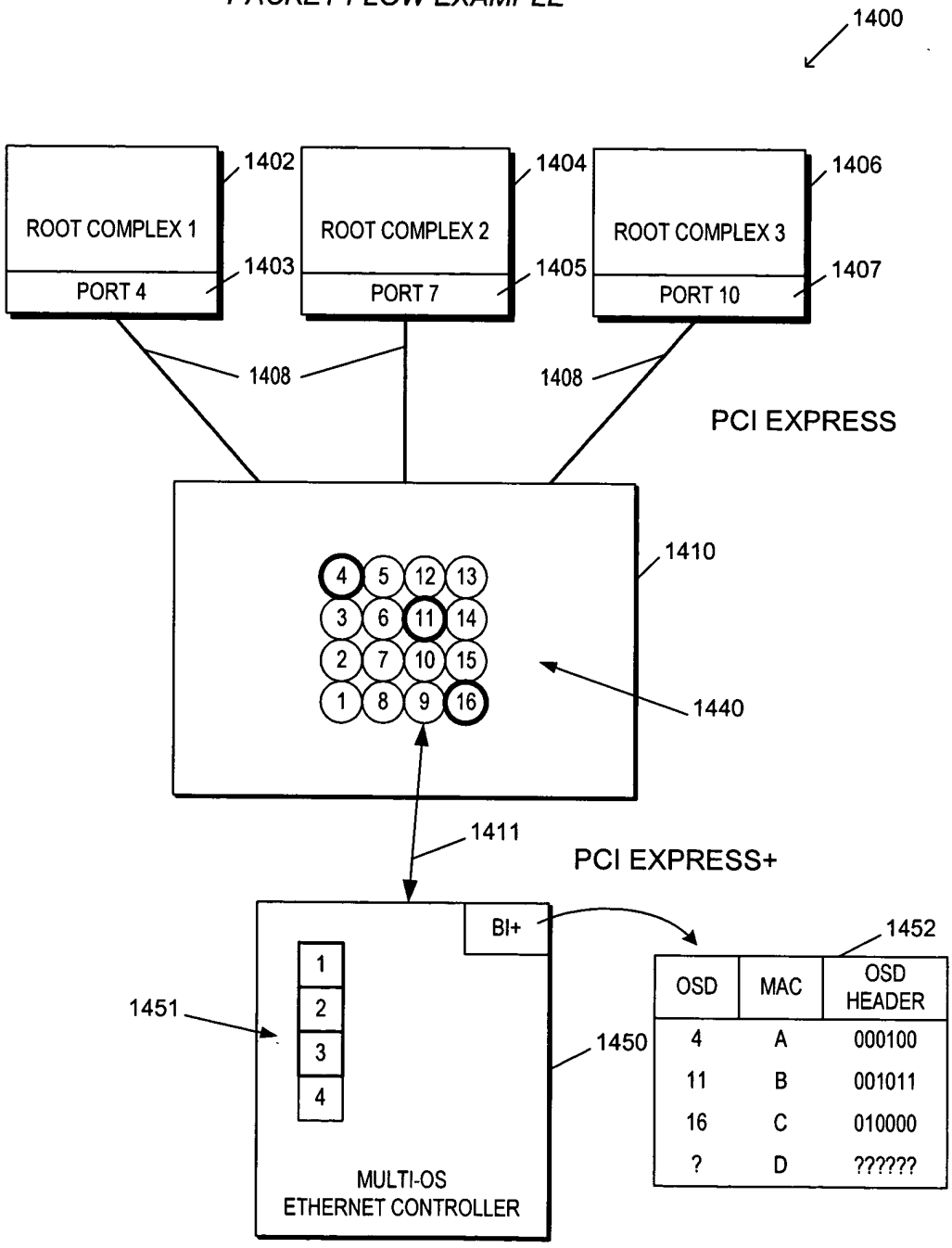


FIG. 15

METHOD OF SHARED I/O DOWNSTREAM TRANSMISSION FROM SWITCH

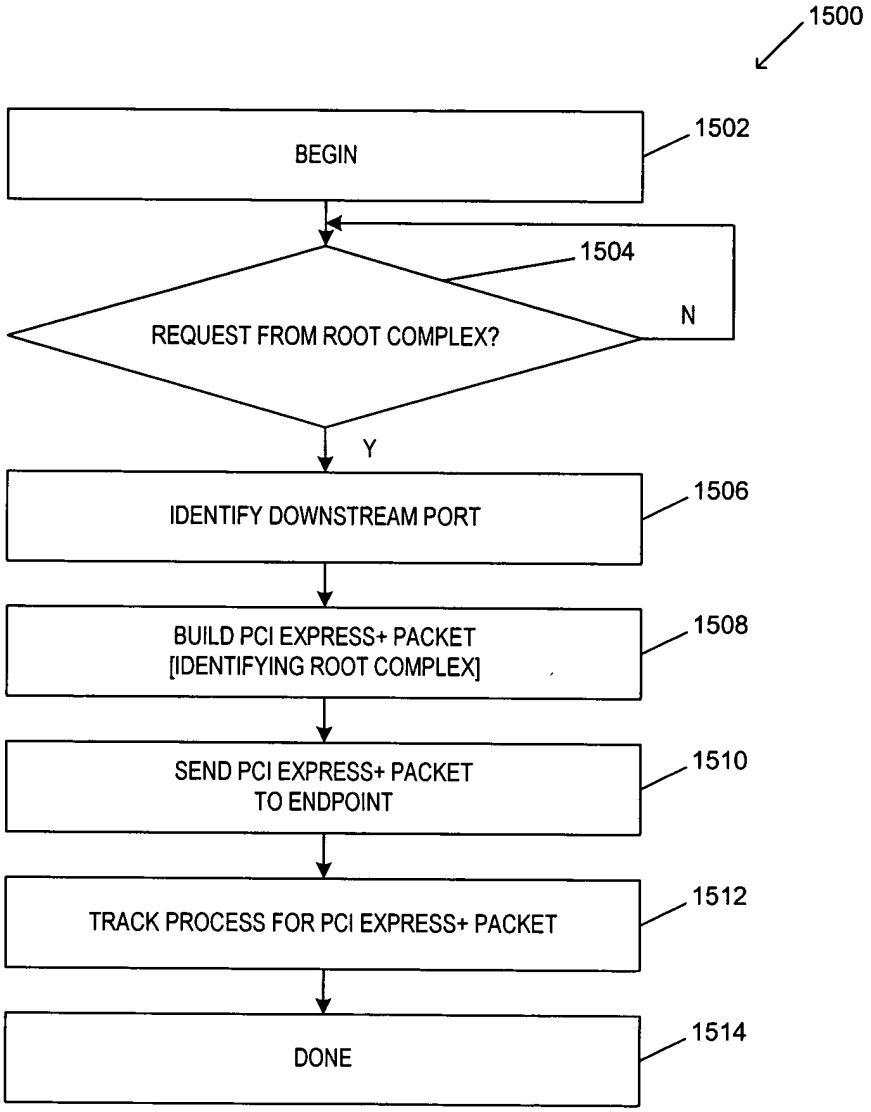


FIG. 16

METHOD OF SHARED I/O UPSTREAM TRANSMISSION TO SWITCH

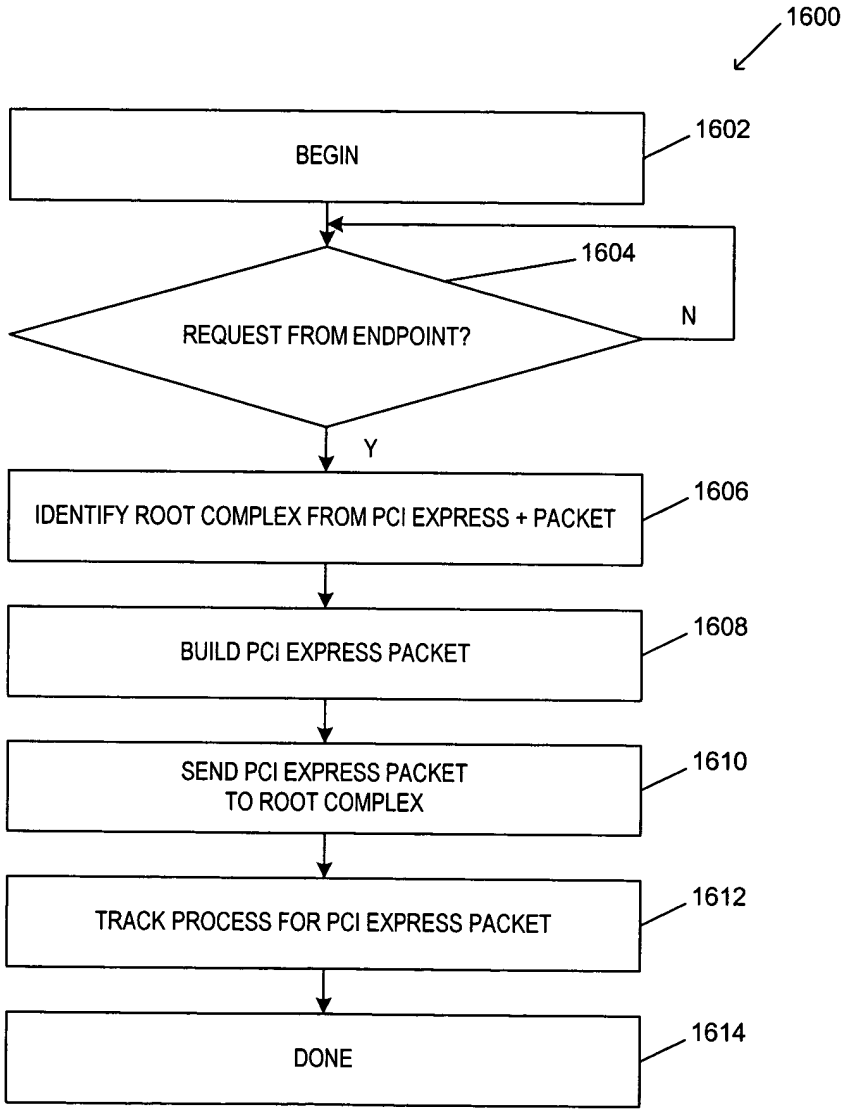


FIG. 17

METHOD OF SHARED I/O DOWNSTREAM TRANSMISSION TO ENDPOINT

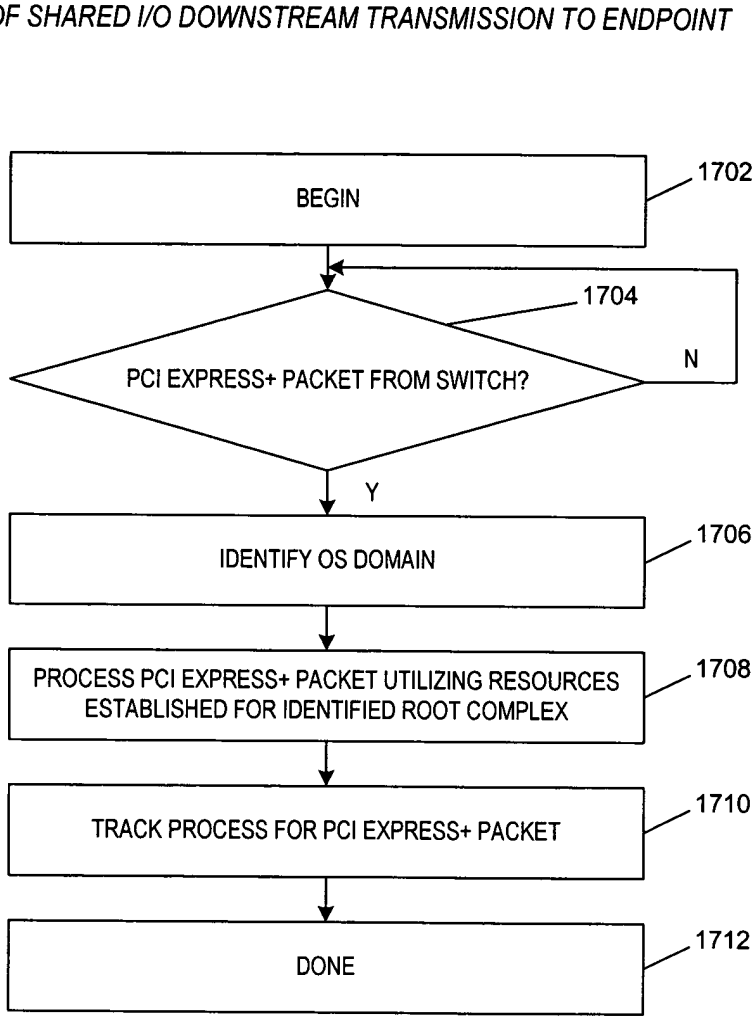


FIG. 18

METHOD OF SHARED I/O UPSTREAM TRANSMISSION FROM ENDPOINT

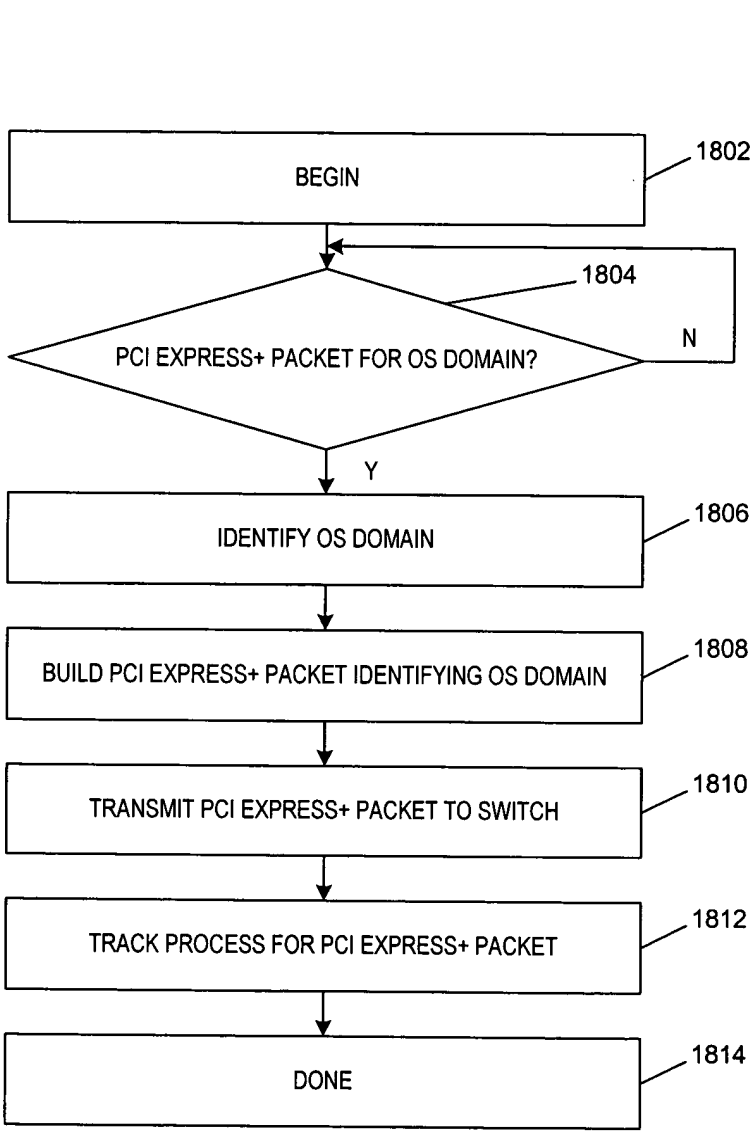
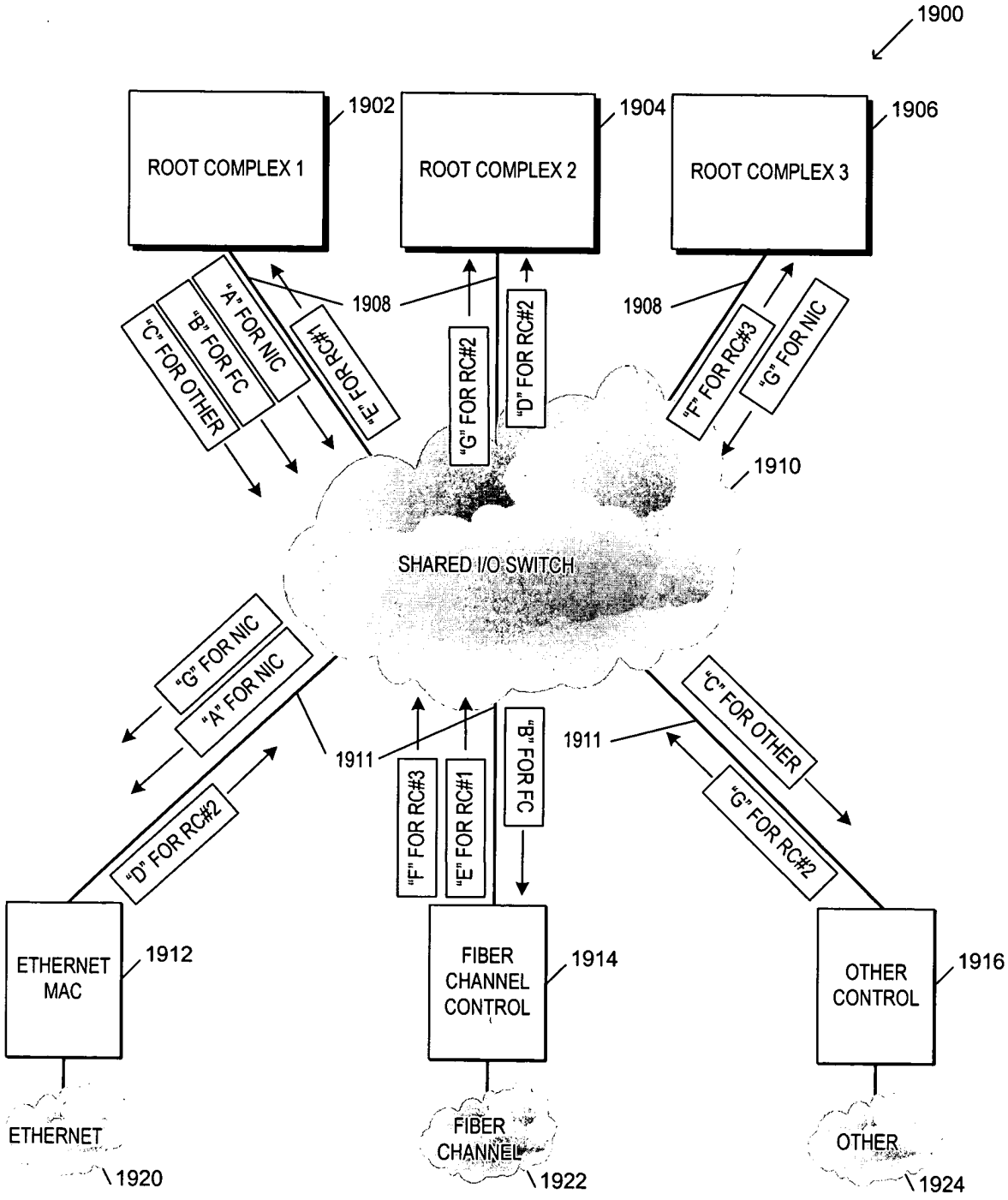


FIG. 19

MULTI-OPERATING SYSTEMS WITH SHARED I/O



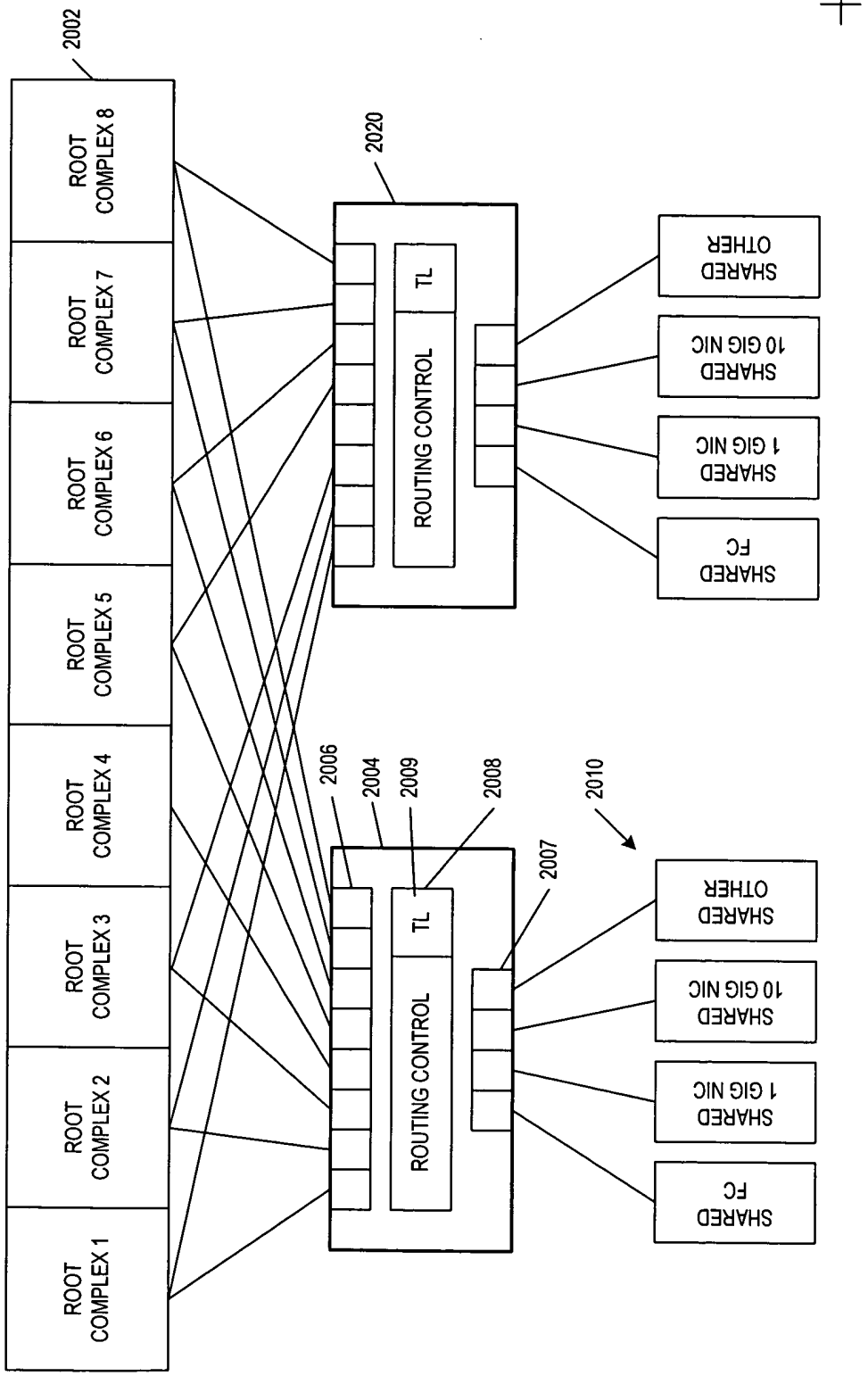


FIG. 20

8 BLADE REDUNDANT ARCHITECTURE WITH SHARED I/O SWITCHES AND ENDPOINTS

FIG. 21

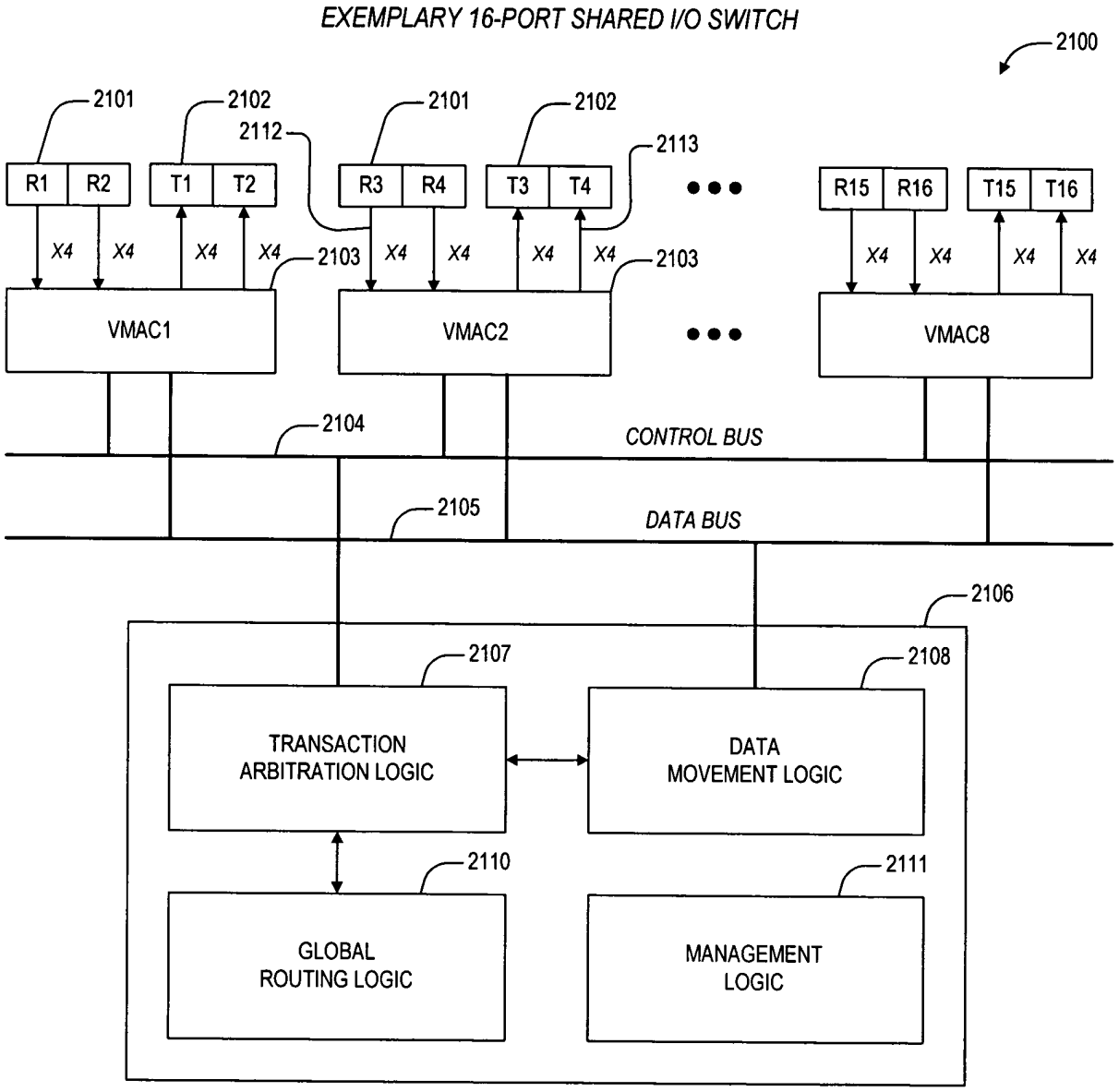
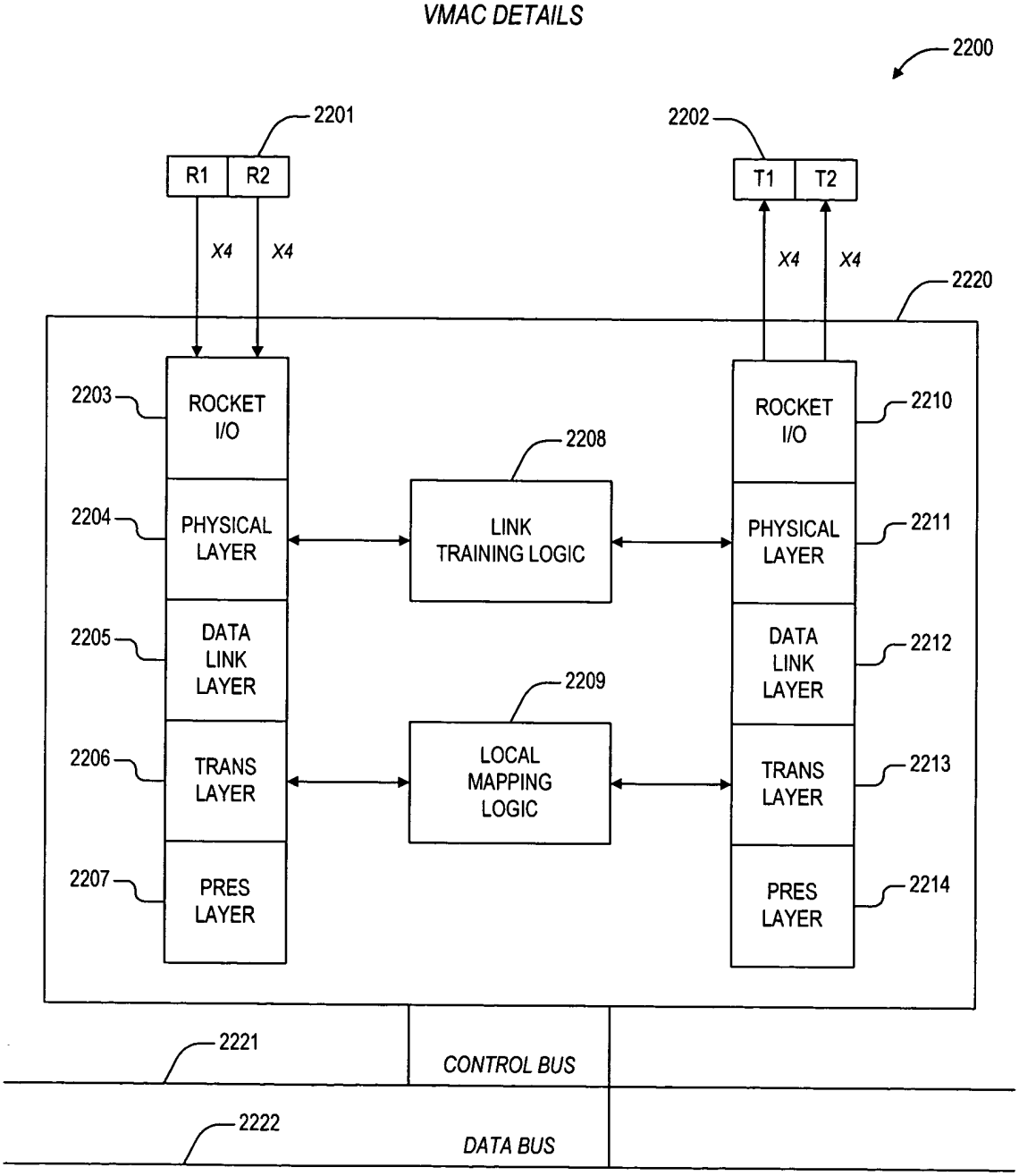

EXEMPLARY 16-PORT SHARED I/O SWITCH
2100
2101
2102
2112
2101
2102
2113
R1
R2
T1
T2
R3
R4
T3
T4
R15
R16
T15
T16
X4
2103
2103
VMAC1
VMAC2
VMAC8
2104
CONTROL BUS
2105
DATA BUS
2106
2107
2108
TRANSACTION ARBITRATION LOGIC
DATA MOVEMENT LOGIC
2110
2111
GLOBAL ROUTING LOGIC
MANAGEMENT LOGIC

FIG. 22


VMAC DETAILS
2200
2201
2202
R1
R2
T1
T2
X4
X4
X4
X4
2220
2203
ROCKET I/O
2210
ROCKET I/O
2208
2204
PHYSICAL LAYER
LINK TRAINING LOGIC
2211
PHYSICAL LAYER
2205
DATA LINK LAYER
2212
DATA LINK LAYER
2209
2206
TRANS LAYER
LOCAL MAPPING LOGIC
2213
TRANS LAYER
2207
PRES LAYER
2214
PRES LAYER
2221
CONTROL BUS
2222
DATA BUS